CLAIMS

What is claimed is:

1. An apparatus for compensating for crosstalk in paths of a backplane, the apparatus comprising:

a first adjuster, coupled to a first path, adapted to adjust a skew of a driver of the first path so as to compensate for crosstalk effects in the first path;

a second adjuster, coupled to the first adjustor, adapted to generate an adjusted replica of the signal in the first path;

a combiner, coupled to the second adjustor, adapted to combine the adjusted replica with a signal of a second path so as to compensate for crosstalk effects in the second path from the signal in the first path; and

a clock synchronization generator adapted to generate a relatively low-speed clock signal,

wherein the relatively low-speed clock signal aligns timing events of a relatively high-speed clock signal that coordinate events in the first and second paths.

2. The invention as recited in claim 1, further comprising:

a third adjuster, coupled to an adjacent channel and the combiner, adapted to generate an adjusted replica of a signal in the adjacent channel, and

wherein the combiner is further adapted to combine the adjusted replica of the signal of the adjacent channel with the signal of the second path so as to compensate for the crosstalk effects in the second path from the signal of the adjacent channel.

3. The invention as recited in claim 1, wherein the signal of the first path is a differential signal, the driver is a differential driver, and the first adjuster is adapted to adjust the positive-to-negative skew of the differential driver.

4. The invention as recited in claim 3, wherein the signal of the second path is a differential signal, and the combiner is a differential subtraction circuit.

5. The invention as recited in claim 1, wherein the clock synchronization generator comprises:

a phase-locked loop (PLL) adapted to generate a high-speed clock signal and a sync signal based on the high speed clock; and

at least one divider, each divider adapted to divide the high-speed clock signal into the low-speed clock signal, and wherein each divider is synchronized to each other divider based on the sync signal.

6. The invention as recited in claim 5, wherein the phase-locked loop (PLL) comprises:

an oscillator generating the high-speed clock signal based on a control signal;

a feedback divider dividing the high-speed clock signal into a feedback signal, the sync signal based on the feedback signal; and

a detector adapted to compare the feedback signal with a reference clock, the control signal based on the comparison of the feedback signal and reference clock.

7. The invention as recited in claim 1, the apparatus is embodied in a circuit.

8. The invention as recited in claim 7, wherein the circuit is an integrated circuit.

9. A method of adjusting signals in one or more transmit paths and one or more receive paths of a backplane, the method comprising the steps of:

(a) adjusting a skew of a driver of a signal of a first path so as to compensate for far-end crosstalk effects in the first path;

(b) generating an adjusted replica of the signal in the first path;

(c) combining the adjusted replica of the signal in the first path with a signal of a second path so as to compensate for near-end crosstalk effects in the second path;

(d) generating a relatively low-speed clock signal; and

(e) aligning, based on the low speed-clock signal, timing events of a relatively high-speed clock signal coordinating events in the first and second paths between the near end and the far end.

10. The invention as recited in claim 9, further comprising the step of repeating steps (a) through (c) so as to iteratively adjust the near- and far-end crosstalk.

11. The invention as recited in claim 9, further comprising:

(f) generating an adjusted replica of a signal in the adjacent channel, and

(g) combining the adjusted replica of the signal of the adjacent channel with the signal of the second path so as to compensate for the crosstalk effects in the second path from the signal of the adjacent channel.

12. The invention as recited in claim 11, further comprising the step of repeating steps (a), (b), (c), (f), and (g) so as to iteratively adjust the signal of the second path.